

NearStack PCIe Connector System and Cable Jumper Assemblies

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NearStack PCIe Connector System and Cable Jumper Assemblies use twinax cables to deliver a PCB alternative and have been optimized for height, PCB density and robustness while enabling implementation of PCIe Gen-5 32-Gbps data rates

Features and Advantages

Built with direct-to-contact twinax termination

Removes the PCB paddle card from the assembly, improving manufacturing efficiencies, repeatability, and signal integrity

Unique contact interface with flexing beams on NearStack cable receptacle

Affords no chance for preloaded beam relaxation through reflow. Has less potential for damage to hard-to-rework PCB side. Offers reduced stub lengths compared to traditional cantilever on PCB pad

Metal housing on plug

- Allows for positive thumb latch interface and solder tail attachment
- Provides rugged, reliable PCB retention

Protected interface

Protects signal pins from “scoop” mating and angled misalignment of up to 6 degrees

Ships with pick-and-place cap

Offers tape-and-reel packaging with pick-and-place cap for seamless integration into a standard PCB assembly process

Right-angle and vertical cable assemblies available

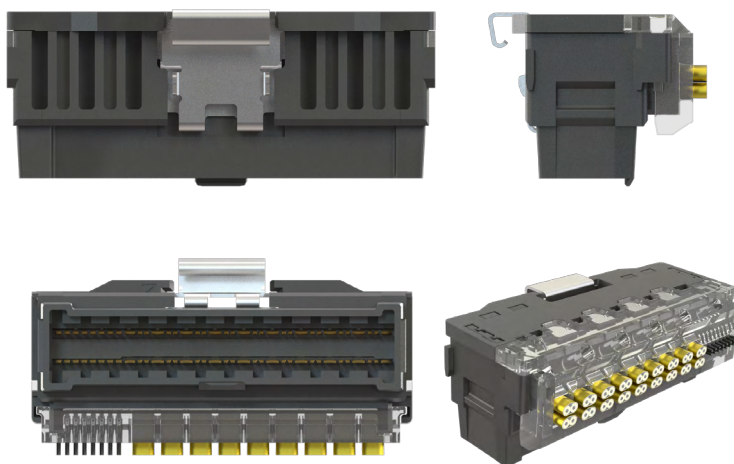
Provides design flexibility with more options for cable routing

Low profile solution

Provides a mated height of 11.10mm (R/A cable) to reduce airflow interference and allow for placement in tighter spaces within the system

Capable of PCIe Gen-5 32-Gbps performance

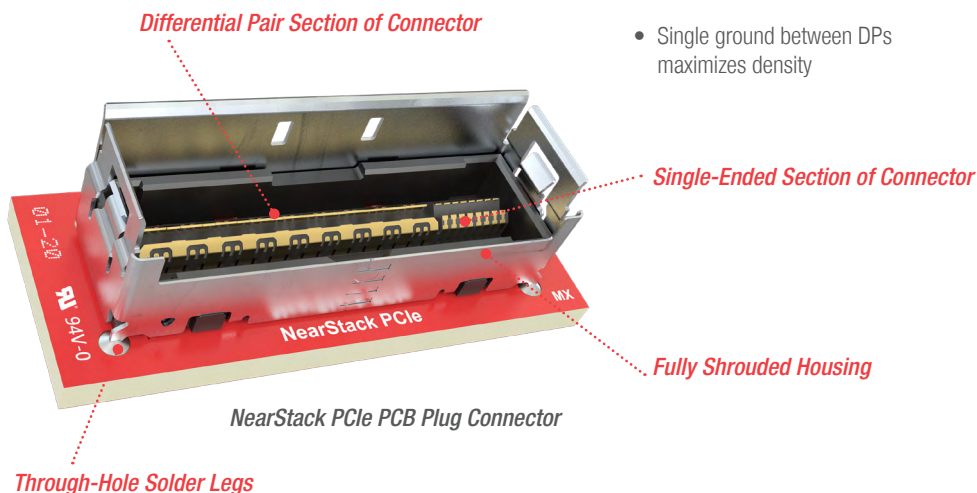
Supports PCIe Gen-5 requirements, with regards to both signal speed (32 Gbps NRZ) and number of pins



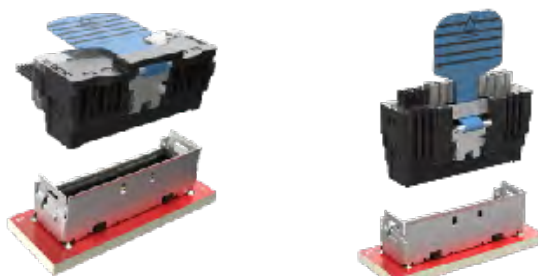
NearStack PCIe Cable Receptacle Connector

x8 version available, which is a single-bay, two-wafer connector

- Delivers 18 differential pairs (GSSGSSG) and 16 single-ended signals (72-pins total)
- Single ground between DPs maximizes density



NearStack PCIe PCB Plug Connector



Right-Angle Cable Assembly

Vertical Cable Assembly

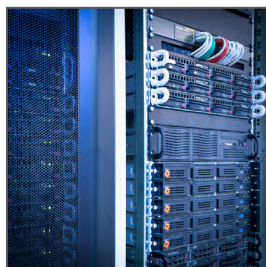
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Markets and Applications

Data Centers

Servers
Storage
High performance computing
Accelerator hardware (graphics, AI)



Data Center Switches

Specifications

REFERENCE INFORMATION

Designed In: Millimeters
RoHS: Yes
Halogen Free: Yes

ELECTRICAL

Voltage (max.): 29.9V RMS
Current (max.): 0.65A (30AWG Twinax) per Mated contact pair, no grouping restrictions
Single Ended Discreet Wire TBD
Contact Resistance: 20 m Ω max Δ (from initial)
Dielectric Withstanding Voltage: 1000V AC RMS
Insulation Resistance: EIA-364-21 1000 Megaohms
Signal Continuity: No interrupts greater than 1 microsecond

MECHANICAL

Mating Force: 2N Max per mated diff pair
Unmating Force: 30N
Durability (min.): 100 Cycles
Wafer Retention force (plug): 1.0N Min per Married wafer set
Normal Force: 30N Min per signal Contact
Mechanical Vibration: EIA-364-28 cond. VII
Mechanical Shock: EIA-364-27 Method A

ENVIRONMENTAL

Temperature Rise: 0.25A thru 8 adjacent ckts with a max temp rise of 30°C
Temperature Life: EIA-364-17 Method A cond. 4
Thermal Shock: EIA-364-32 Method A cond. I
Cyclic Temperature and Humidity: EIA-364-31 Method III
Mixed Flowing Gas: EIA-364-65 Class IIA Option 2
Thermal Disturbance: EIA-364-110 Cond A duration A
Dust: EIA-364-91

PHYSICAL

Plug Housing: LCP
Plug Shell: Stainless steel
Plug Wafers: LCP & Copper Alloy
Plug Vacuum Cap: LCP
Receptacle Housing: LCP
Receptacle Wafers: LCP & Copper Alloy
Receptacle Cover: LCP
Receptacle Top Retainer: Polycarbonate (clear)
Receptacle Bottom Retainer: Polycarbonate (clear)
Receptacle Latch: Stainless Steel
Receptacle Protective Cover: Polypropylene (PMS Blue 2192C)
Contact: Copper (Cu)
Plating:
Contact Area — 0.76 μ (30 μ ") over 1.72 μ Nickel overall
SMT Tail Area — 2.54 μ Selective Tin (Sn) over 1.27 μ (50 μ ") Nickel (Ni) Overall
Operating Temperature: -40 to +85°C

www.molex.com/link/nearstack.html

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